A guide to 1.6T Ethernet

EXFO

1 Highlights: IEEE 802.3dj standard

Addresses needs of hyperscale data centers, and AI infrastructure.

FFE DFE

Enhanced transmitter and receiver equalization improves signal integrity over challenging high-speed channels.

200G

Defines the transition to 200G-per-lane technology, enabling 1.6TbE systems and also supporting 200G, 400G, and 800G running at 200G per lane.

APSU

Defines autonomous path startup (APSU) process facilitated by the ILT and RTS functions.

1.6T

Defines per-lane 200 Gbit/s physical layer and MAC for 1.6 Tb/s aggregated interfaces.

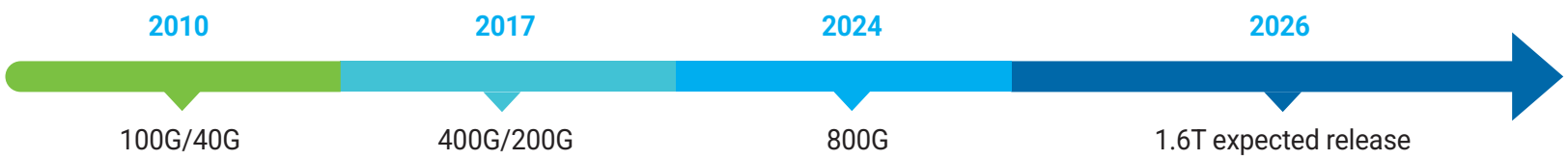
RS-FEC

Introduces RS-FEC symbol multiplexing to multiplex symbol pairs or symbol quartets.

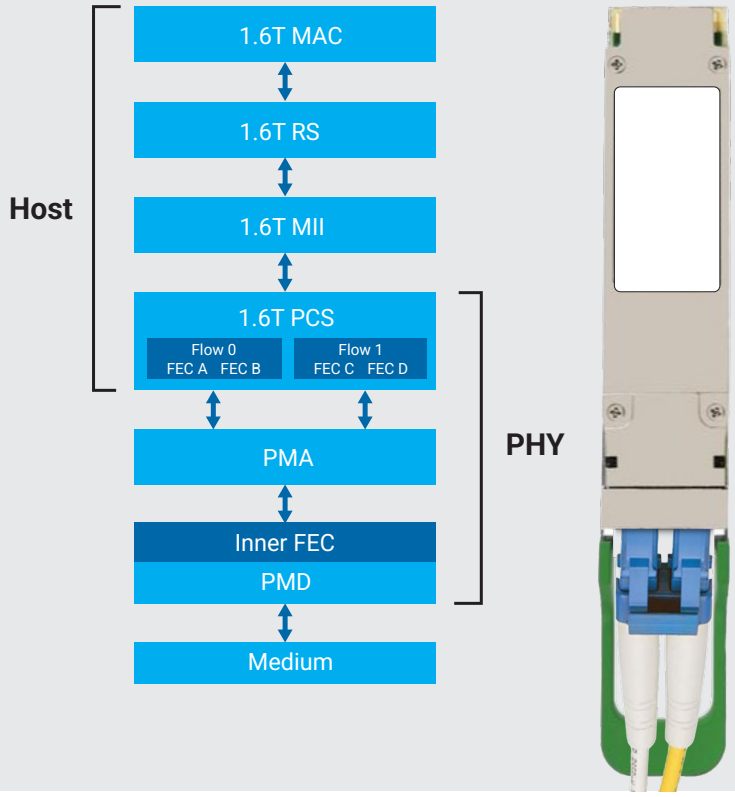
Leverages PAM4 signaling across electrical and optical interfaces to achieve 200 Gbit/s per lane.

Defines an additional forward error correction (FEC) layer, known as Inner FEC, for selected longer-reach applications

Timeline: Ethernet standard



2 1.6TE layer by layer



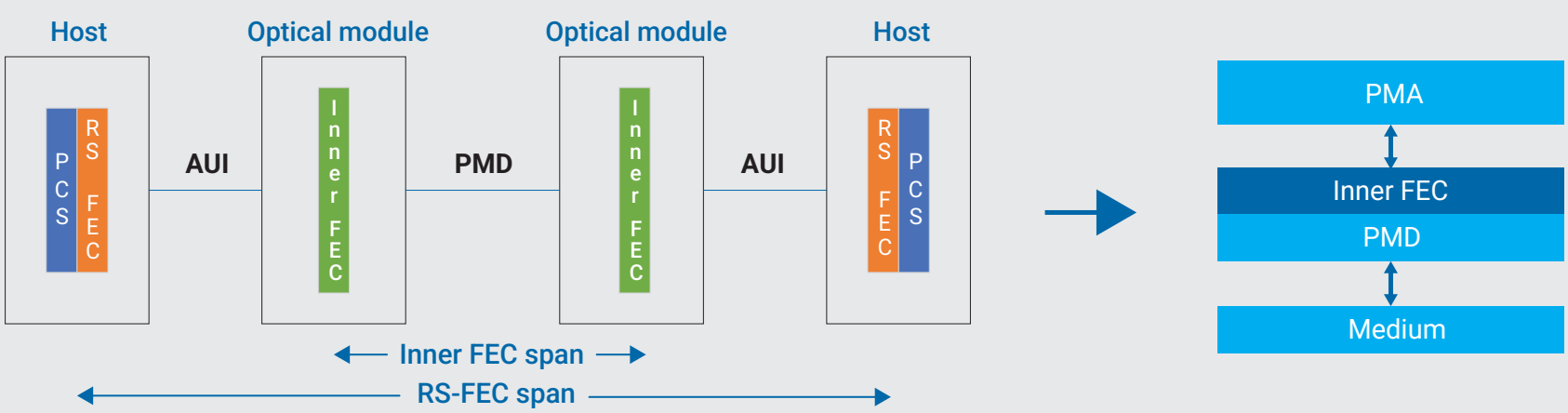
LEGEND	
MAC	Media access control
RS	Reconciliation sublayer
MII	Media independence interface
PCS	Physical coding sublayer
PMA	Physical medium attachment
PMD	Physical medium dependent
FEC	Forward error correction

3 Inner FEC

For 2 km and 10 km interfaces, the 1.6T standard mandates the implementation of an additional forward error correction (FEC) layer, referred to as the inner FEC, in addition to the RS-FEC implemented in the PCS layer.

Key characteristics include:

- RS-FEC: remains an end-to-end FEC mechanism and is not terminated at any intermediate sublayer.
- Inner FEC: implemented within the physical medium dependent (PMD) layer, meaning it resides directly inside the optical module.
- Inner FEC specification is defined in clauses 177 and 183 of the standard.
- Dual-FEC architecture enhances link robustness for higher-speed optical interfaces while preserving end-to-end error correction through the PCS RS-FEC.



4 PMA: symbol multiplexing

What is symbol multiplexing?

A symbol is a group of bits that represents a coded value. In IEEE 802.3 Ethernet PHYs, data is organized into symbols rather than individual bits after encoding and FEC processing.

As Ethernet scales to 1.6 Tb/s with 200 Gbit/s electrical lanes, bit multiplexing becomes increasingly difficult to implement at the required speeds.

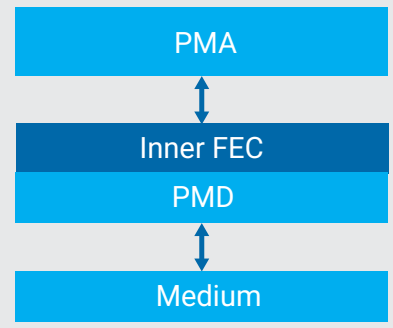
The advantages of symbol multiplexing:

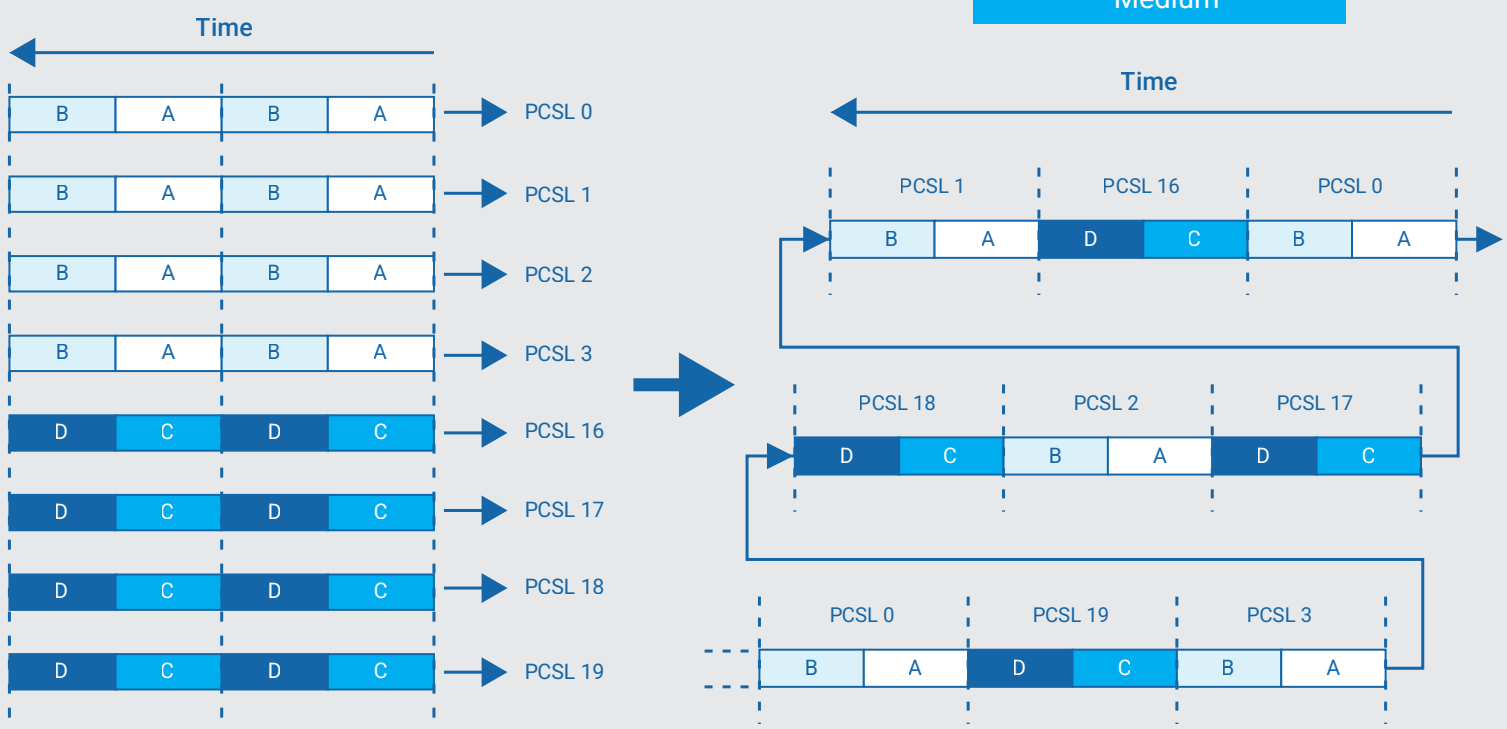
- Bit mux: interleaves data one bit at a time from multiple lanes.
- Symbol mux: interleaves data one complete symbol at a time, keeping all the bits of a symbol together.

For example:

```
Bit mux: Lane 0: 1010... Lane 1: 1101...
Output: 1 1 0 1 1 0 0 1 ...
Symbol mux (4-bit symbols):
Lane 0: [1010] [0011]
Lane 1: [1101] [0100]
Output:
[1010] [1101] [0011] [0100]
```

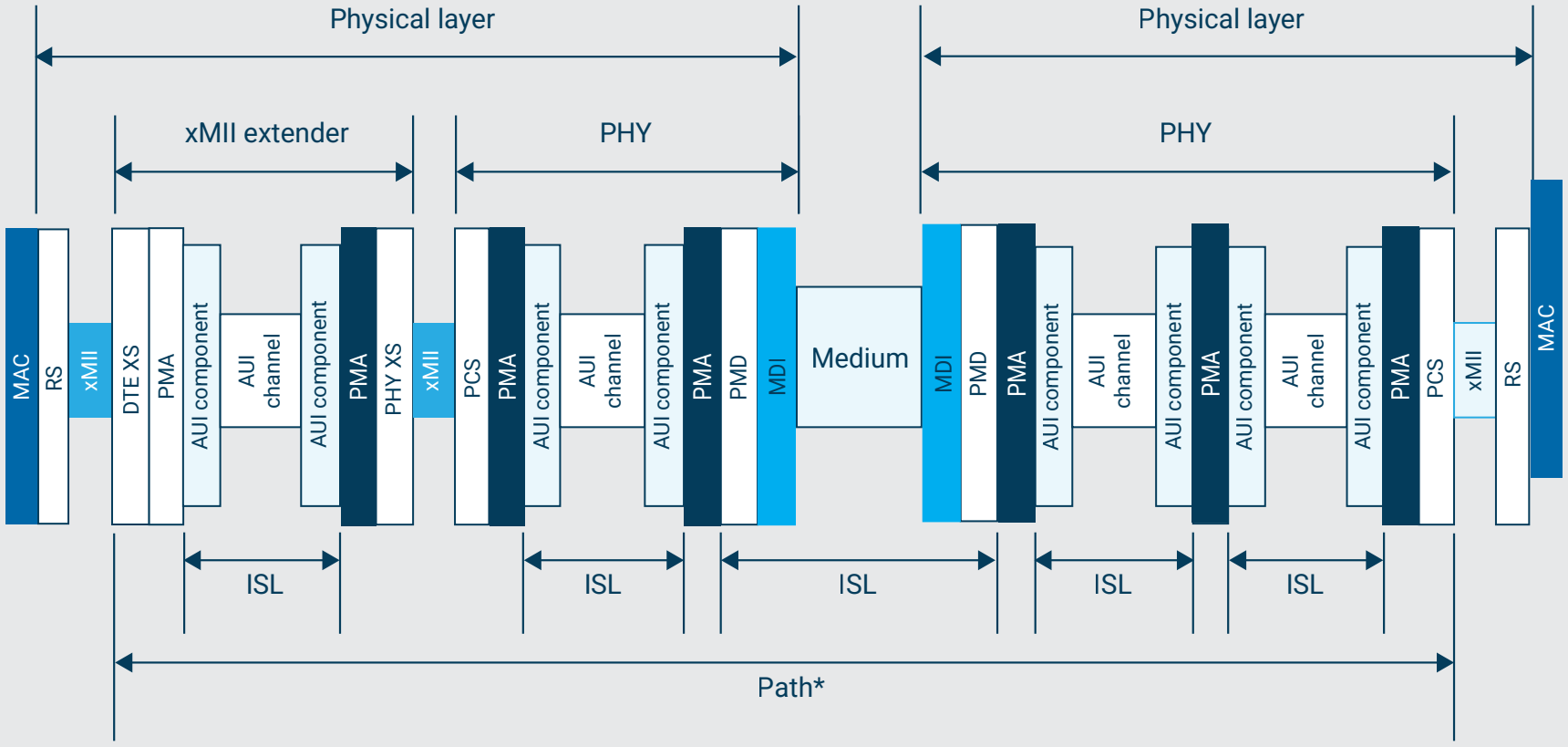
- Lower implementation complexity: entire symbols are switched instead of individual high-speed bits, simplifying the hardware.
- Better timing alignment: symbol boundaries are preserved, reducing skew and synchronization challenges between lanes.
- Improved compatibility with FEC: since forward error correction operates on symbols, keeping symbols intact simplifies encoding and decoding.
- Higher-speed scalability: symbol MUX is more practical for 200 Gbit/s per-lane operation and future Ethernet speeds.





5 Autonomous path startup (APSU)

- IEEE 802.3 Clause 72 (802.3ap-2007) first introduced the concept of Link Training, a startup process in which the receiver tunes the remote transmitter's equalization settings to maximize signal quality. Subsequent IEEE amendments expanded Link Training to support higher speeds and additional electrical interfaces.
- Building on decades of Link Training evolution, IEEE P802.3dj evolves Ethernet startup capabilities for interfaces that include one or more Inter-Sublayer Links (ISLs) operating at 200 Gbit/s per lane and higher.
- Rather than treating transmitter training as a standalone function, Annex 178B of the draft introduces Autonomous Path Startup (APSU), a framework that coordinates startup across an entire communication path. APSU provides coordinated, orderly initialization of all links and sublayers in a path rather than focusing solely on a single transmitter-receiver pair.
- APSU is enabled through two complementary functions:
  - ILT (Inter-Sublayer Link Training) — establishes communication across an individual ISL and performs the training functions needed to bring that connection into service.
  - RTS (Ready-to-Send) — propagates startup readiness and coordinates activation across a series of ISLs along the end-to-end path.
- Together, ILT and RTS enable APSU to bring complex 200G-per-lane Ethernet paths into operation in a coordinated and deterministic manner.



*RTS and/or ILT performed on each ISL in the end-to-end path

6 Physical-layer specifications

DATA RATE	PHY TYPE	INNER FEC	OPTICAL MODULATION	MEDIA LANES	REACH
200 Gbit/s	200GBASE-CR1	-	-	1x Copper	-
	200GBASE-DR1	-	PAM4	1x SMF	500 m
	200GBASE-DR1-2	√	PAM4	1x SMF	2 km
400 Gbit/s	400GBASE-CR2	-	-	2x Copper	-
	400GBASE-DR2	-	PAM4	2x SMF	500 m
	400GBASE-DR2-2	√	PAM4	2x SMF	2 km
800 Gbit/s	800GBASE-CR4	-	-	4x Copper	-
	800GBASE-DR4	-	PAM4	4x SMF	500 m
	800GBASE-DR4-2	√	PAM4	4x SMF	2 km
	800GBASE-ER1	-	DP-16QAM	1x SMF (Coherent)	40 km
	800GBASE-ER1-20	-	DP-16QAM	1x SMF (Coherent)	20 km
	800GBASE-FR4	√	PAM4	1x SMF (4λ)	2 km
	800GBASE-FR4-500	-	PAM4	1x SMF (4λ)	500 m
	800GBASE-LR1	√	DP-16QAM	1x SMF (Coherent)	10 km
	800GBASE-LR4	-	PAM4	1x SMF (4λ)	10 km
1.6 Tbit/s	1.6TBASE-CR8	-	-	8x Copper	-
	1.6TBASE-DR8	-	PAM4	8x SMF	500 m
	1.6TBASE-DR8-2	√	PAM4	8x SMF	2 km

Note: IEEE 802.3dj defines two Inner FEC architectures: Clause 177 for DR-x-2 PHYs and Clause 184 for 800GBASE-LR1.

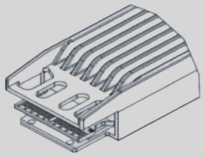
7 Interfaces

The main interfaces at 1.6T are using the form factor octal small-form-factor pluggable (OSFP).

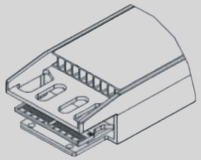
Currently there are two main varieties:

OSFP-IHS

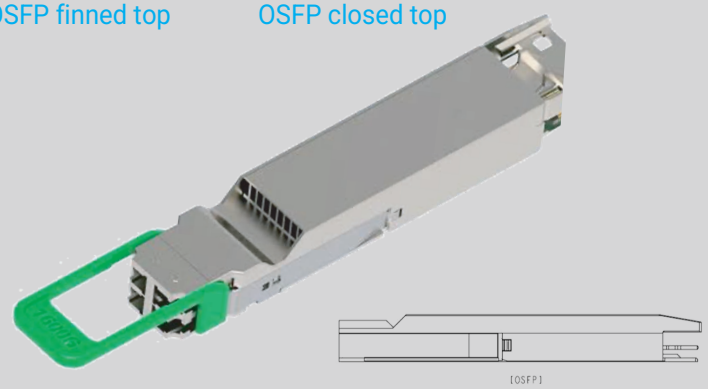
Integrated heat sink



OSFP finned top

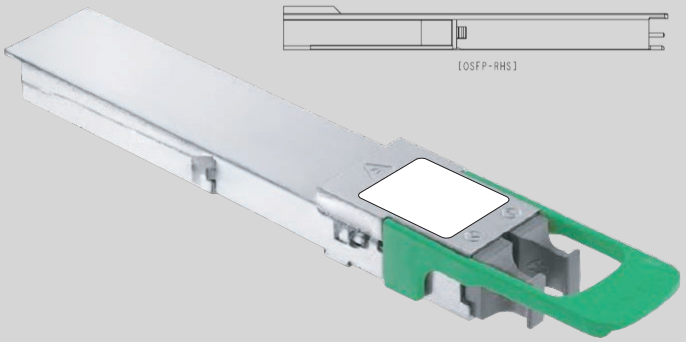


OSFP closed top



The OSFP integrated heat sink (IHS) incorporates the heat sink directly into the optical module. This self-contained design enables efficient air cooling at 1.6T. Available in both closed finned top and open finned top configurations.

OSFP-RHS



The OSFP riding heat sink (RHS) uses a host-mounted heatsink that interfaces with the module's flat-top surface, combining enhanced thermal performance with high faceplate density to support emerging 1.6T optical modules.

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