

BA-1600

1.6T BIT ANALYZER

- World-class, high-performance electrical BER tester for 1.6T design validation, including thermal testing.



KEY FEATURES

Full lifecycle validation for 1.6T, 800G and 400G across lab, fab and live environments

Superior hardware design: native electrical interface, excellent signal quality, clean eye diagram and low error floor

High-performance signal integrity and BER testing for validating compliance and performance in next-gen 1.6T designs

Flexible, cost-effective: choose 8-channel unit for transceiver testing, or 4-channel unit for high-speed component testing

User-friendly GUI streamlines workflows, and reduces learning curves

PAM4 support for validating high-speed signaling performance

FEC generation and analysis testing to ensure data integrity over ultra-fast connections

Real-time FEC analysis: testing of pre/post FEC BER, symbol error distribution and FEC margin

BLER: Block error ratio statistics and an efficient FLR estimation mechanism, addressing the time constraints of ultra-low BER measurements

Powerful equalizer and channel simulator: powerful equalizer includes CTLE

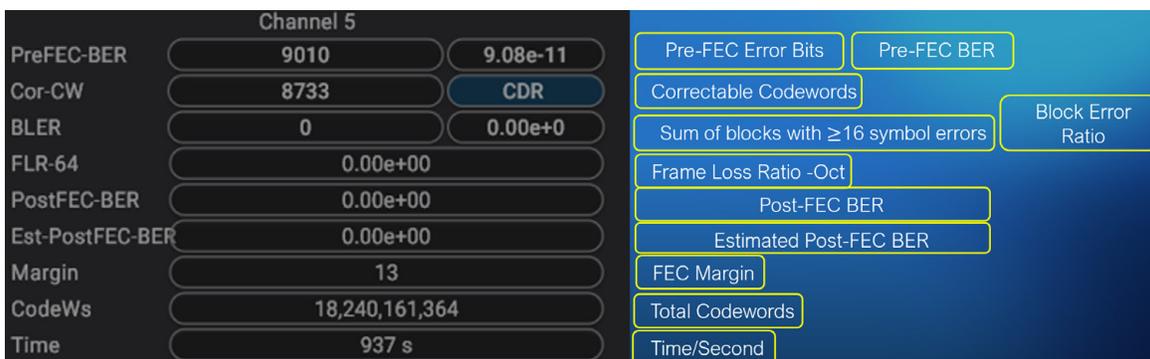
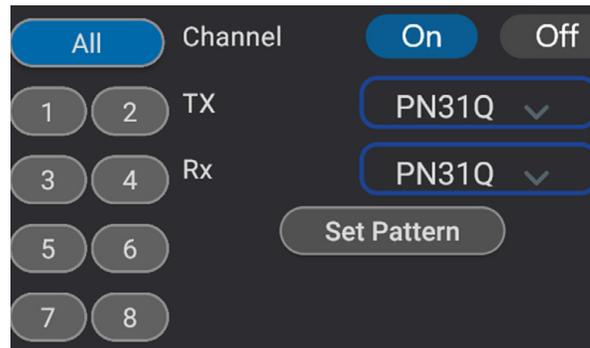
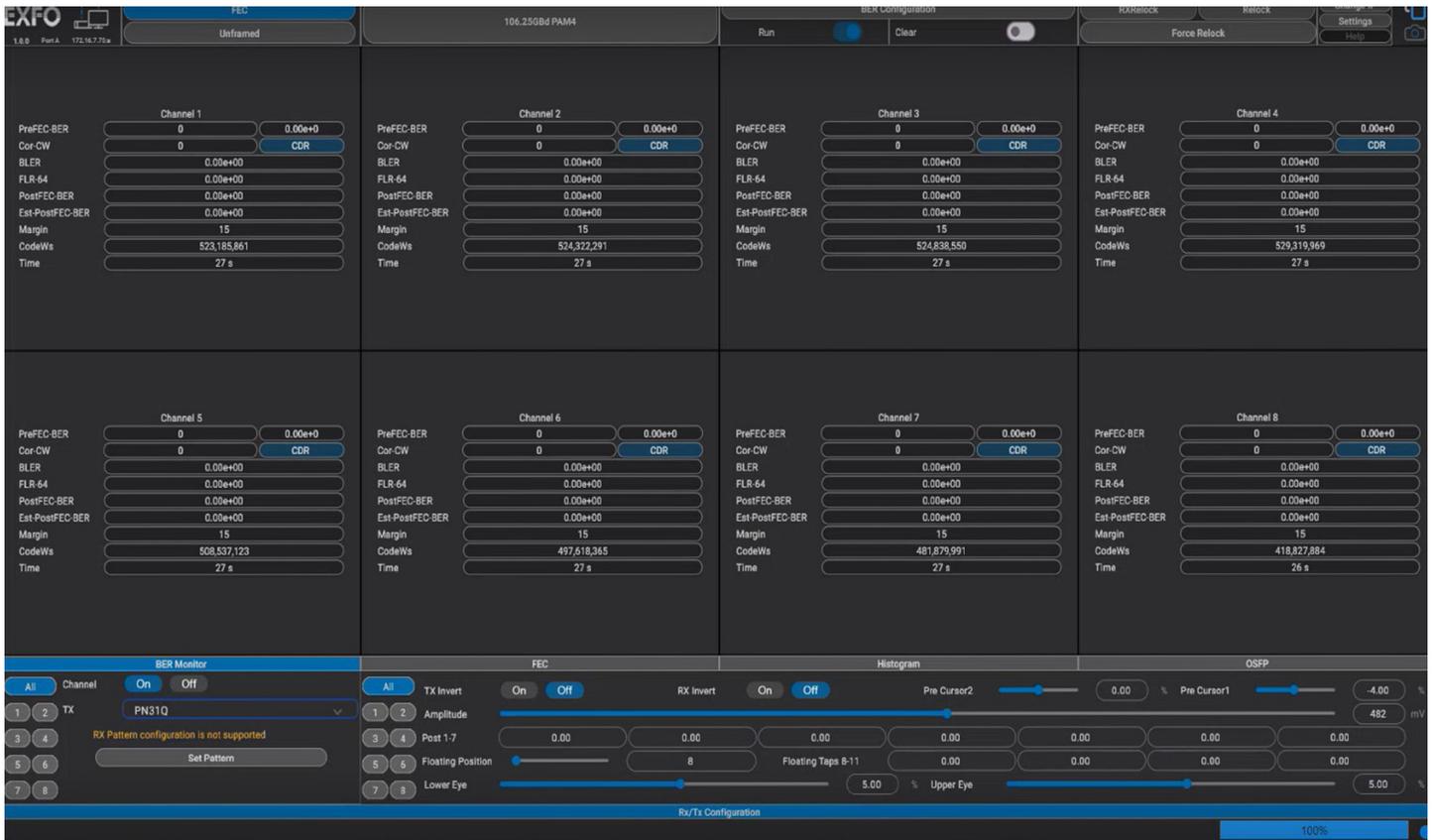
I²C register read/write access enables the direct control and monitoring of device parameters for fast, low-level diagnostics and efficient debugging

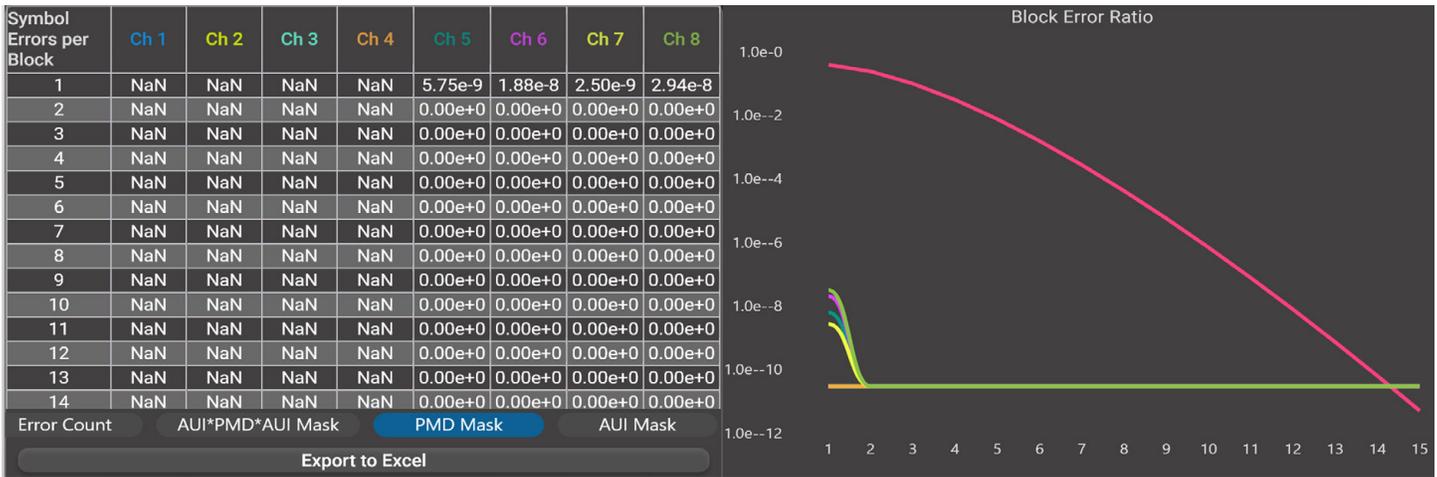
“Save-and-load” functionality for all applicable parameters reduces valuable time and ensures test consistency

Automation simplifies complex test configurations and speeds up validation using a complete API suite

POWERFUL AND SIMPLIFIED USER INTERFACE

The BA-1600 graphical user interface (GUI) provides simplified and real-time test results per channel. It requires an external Windows-based PC with Ethernet capability to run the GUI and API.





FEC channel distribution and BLER mask testing

Board Type: OSFP QSFPDD

Power Supply: V

HW Signals: LPWn RSTn PRSn Int High(3.3v) Low(ground)

I2C register: Address Value R W

MCB control

Clock Ratio: Rate/2 Rate/4 Rate/8 Rate/16 Rate/32

Enable output Clock: Channel 5 Channel 6 Channel 7 Channel 8

Clock output Channel: Channel 1 Channel 2 Channel 3 Channel 4 Channel 5 Channel 6 Channel 7 Channel 8 CDR: BER: Errors: Sync: # Bits: # Bits: # Bits: # Bits: Time: Time: Time: Time:

Reference clock

WITH PAM4 CODING, A SIMPLE BER TEST IS NOT ENOUGH

Channel 1

Pre-FEC-BER:

Cor-CW:

CER:

FLR-64:

Est-CER:

Est-FLR:

Margin:

CodeWs:

Time:

FEC symbol error margin

BA-1600 Application

EXFO 106.25Gb/s PAM4

Unframed Clock Rate: 8

BER Configuration: Run Clear Force Rclock Settings Help

Number of Symbols	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7	Ch 8
1	0	0	0	0	10	33	3	64
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0

Error Count: AUI*PMD*AUI Mask PMD Mask AUI Mask

BER Monitor: Channel All TX Invert RX Invert Invert Dcursor2: 0.00 % Pre Cursor1: -4.00 %

Amplitude: mV

Post 1-7:

Floating Position:

Floating Taps 8-11:

Lower Eye: Upper Eye:

FEC symbol error distribution plot

BA-1600 Application

EXFO 106.25Gb/s PAM4

Unframed Clock Rate: 8

BER Configuration: Run Clear Force Rclock Settings Help

SNR:

Slicer:

Thid:

Thid:

Thid:

Histogram Mon: Sequential Concur

Scale: Linear Lo

BER Monitor: Channel All TX Invert RX Invert Invert Dcursor2: 0.00 % Pre Cursor1: -4.00 %

Amplitude: mV

Post 1-7:

Floating Position:

Floating Taps 8-11:

Lower Eye: Upper Eye:

Error Injection: 100%

Channel histogram

BER Monitor: Channel All TX Invert RX Invert Invert Dcursor2: 0.00 % Pre Cursor1: -4.00 %

Amplitude: mV

Post 1-7:

Floating Position:

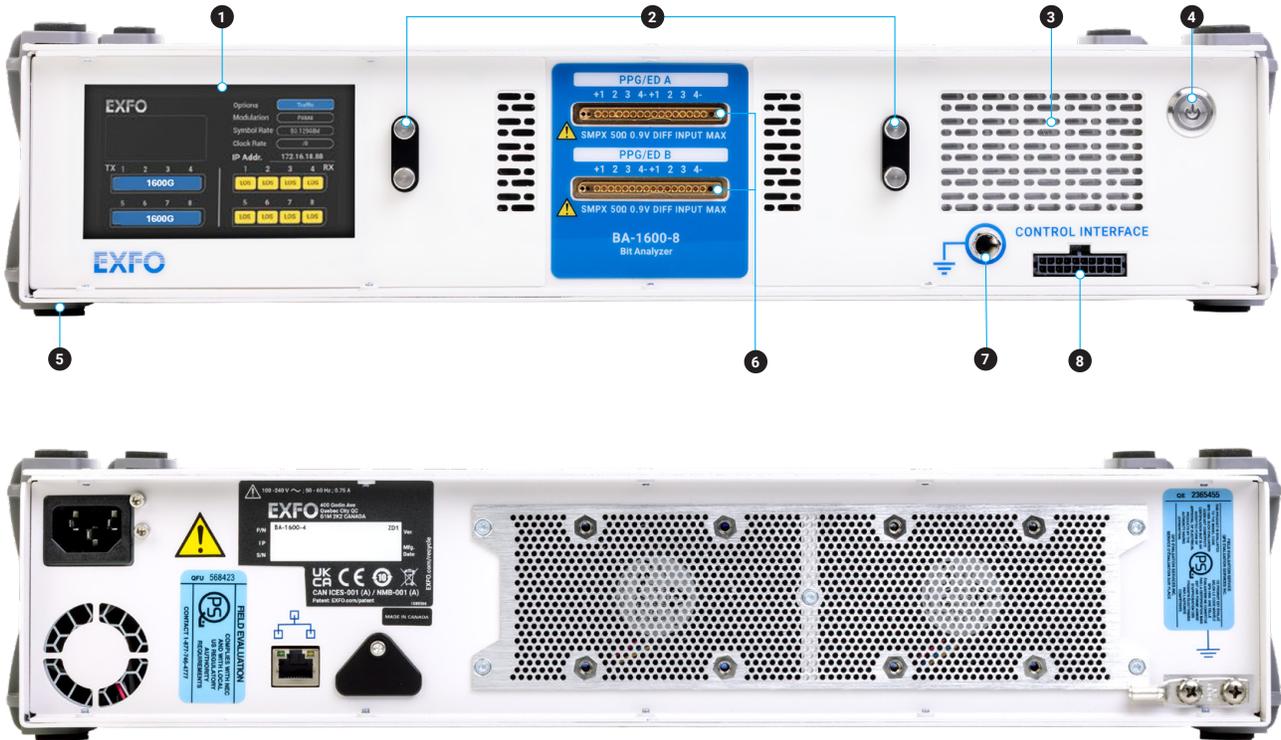
Floating Taps 8-11:

Lower Eye: Upper Eye:

14-tap mode

DESIGNED FOR HIGH-SPEED AND MULTISERVICE

- 1 Display 4.5 inch
- 2 MCB support bracket mount (optional)
- 3 Air inlet
- 4 Power button
- 5 Foot rest
- 6 RF user connectors (SMPX)
- 7 Grounding jack
- 8 MCB interface connector



SPECIFICATIONS

SPECIFICATIONS	
Number of channels	8 or 4
Data rate per lane (GBd)	106.25, 53.125 and 26.5625
Data rate adjustment (ppm)	±250
PAM4 coding	Gray code
Pattern supported by PPG and ED	PPG: PRBS 7Q/9Q/10Q/11Q/13Q/15Q/20Q/23Q/31Q/49Q/58Q/SSPRQ/SQUARE_WAVE ED: PRBS 7Q/9Q/10Q/11Q/13Q/20Q/23Q/31Q/49Q/58Q ^a
PG maximum amplitude (mV _{ppd})	900
Jitter RMS (mUI)	≤23
EOJ03 (mUI)	≤25
JH4u (mUI)	≤135
ED maximum level (mV _{ppd})	1200
ED damage level (mV _{ppd})	1300
TX multi tap pre-emphasis support	10 fix taps + 4 floating taps ^b
Rx sensitivity (mV _{ppd})	≥300 ^c
Connector type	SMPX 1x16

GENERAL SPECIFICATIONS

Size (H × W × D)	115 mm × 465 mm × 300 mm (4.5 in × 18.3 in × 11.8 in)
Weight	≤ 10 kg (22 lb)
Temperature	Operating: 5 °C to 40 °C (41 °F to 104 °F) Storage: -20 °C to 70 °C (-4 °F to 158 °F)
Relative humidity	20% to 80%
Power	100 Vac to 240 Vac (47 Hz to 63 Hz) 55 W typical / 80 W max.

MODULE COMPLIANCE BOARD (MCB)

Part number	EXFO- Wilder WMCB-OSFP-1.6T MCB SMPX-to-SMPX
Interface	OSFP1600 support
Direct SMPX connection	BA-1600-8 and BA-1600-4
Power class	Class 4 and higher pluggable with cooling system
CMIS	CMIS control and I ² C read/write

a. Only 13Q, 20Q, 23Q, 31Q, 49Q, 58Q patterns are supported in RX at 106.25 GBaud.

b. Max 14 UI away from fix taps.

c. BER <e-11 for the below channel conditions:
 - BA TX → 150mm Cable → Junction → 150mm Cable → BA RX
 - Optimal Transceiver tuning for the channel is applied
 - BA TX mV amplitude is then decrease from 900mV until BER hit e-11 (PRBS31Q)



ACCESSORIES

GP-3273	RF loopback cable SMPX to SMPX 1×16 (qty: 1)
GP-3274	RF fanout cable SMPX 1×16 to V 1.85 mm male (length = 15 cm) (qty: 1)
GP-3275	RF fanout cable SMPX 1×16 to V 1.85 mm male (length = 30 cm) (qty: 1)
GP-3276	BA-1600 MCB cable assembly (this is the low-speed CMIS control cable) (qty: 1)
GP-3277	19" relay rack mounting bracket + screws/HW



GP-3273



GP-3274



GP-3275



GP-3276

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